III-V CMOS: *Quo Vadis?*

J. A. del Alamo, X. Cai, W. Lu, A. Vardi, and X. Zhao

Microsystems Technology Laboratories

Massachusetts Institute of Technology

Compound Semiconductor Week 2018

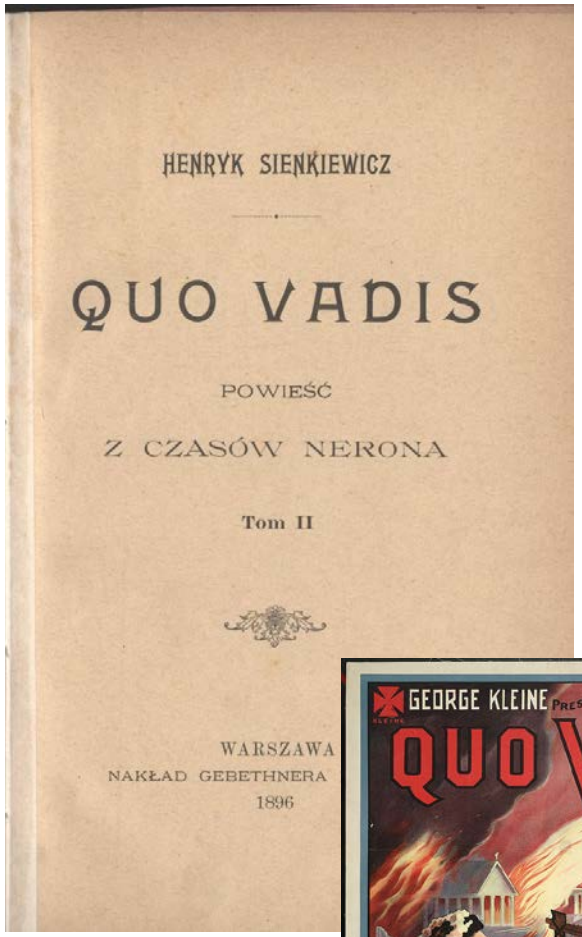
Cambridge, MA, May 29-June 1, 2018

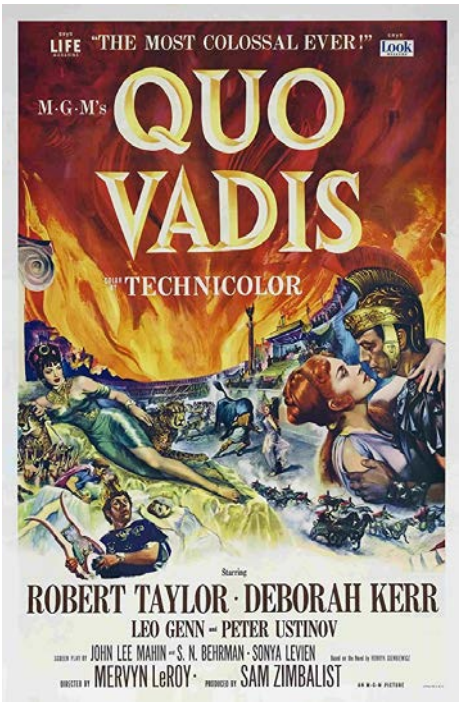
Acknowledgements:

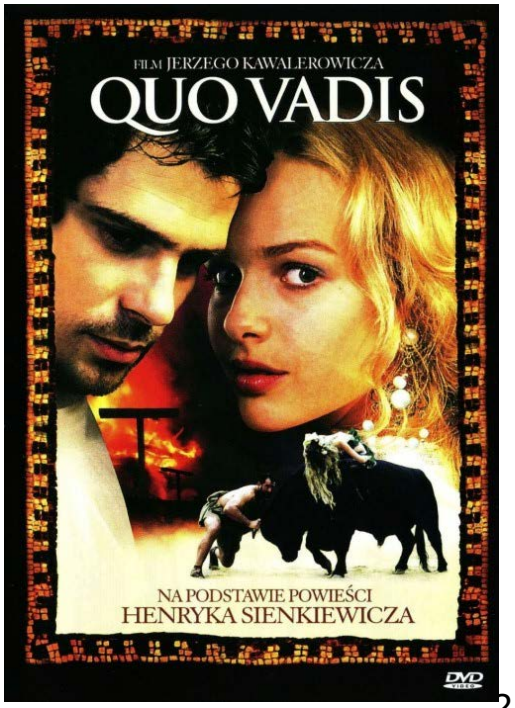
- Former students and collaborators: D. Antoniadis, E. Fitzgerald, J. Grajal, J. Lin
- Sponsors: Applied Materials, DTRA, KIST, Lam Research, Northrop Grumman, NSF, Samsung, SRC
- Labs at MIT: MTL, EBL

Quo Vadis? =

Where are you going?



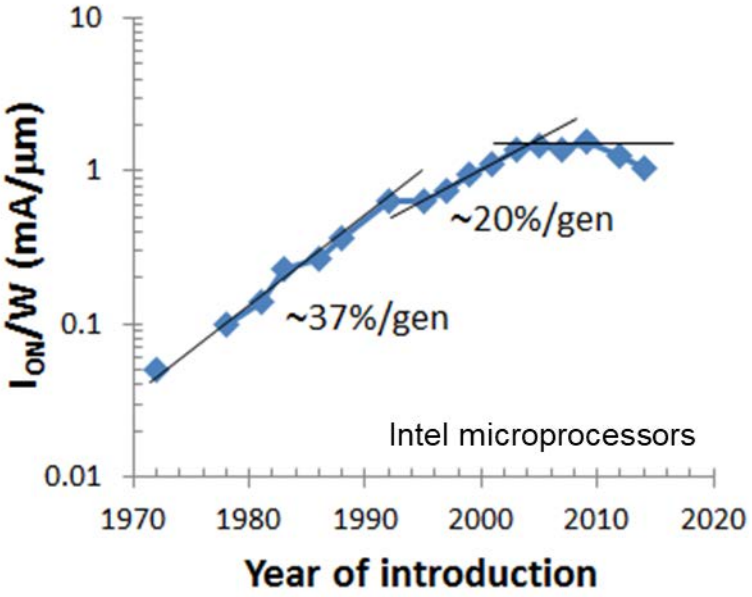




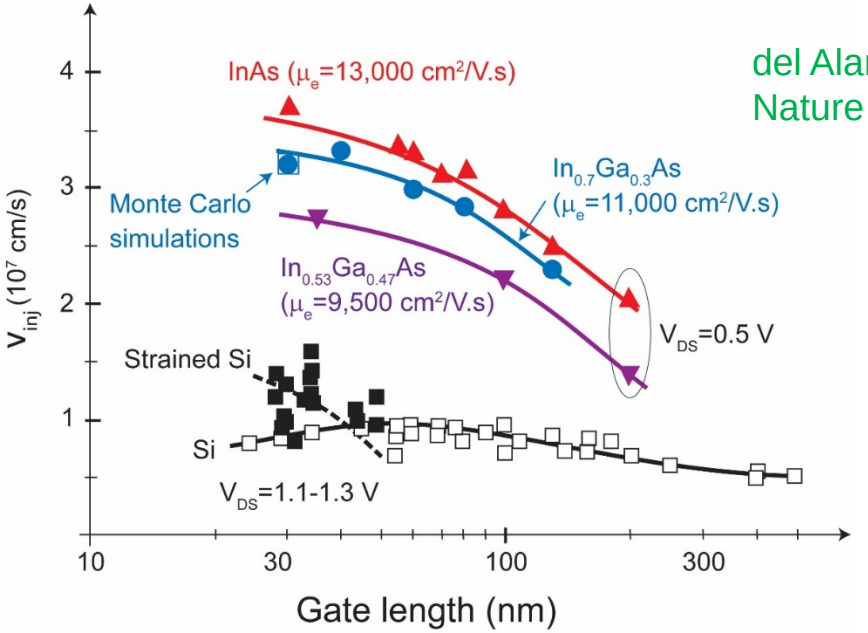
III-V CMOS: The Promise

Scaling: Voltage ↓ → Current density ↓ → Performance ↓

Current density of n-MOSFETs at nominal voltage:



Source injection velocity: Si vs. InGaAs FETs

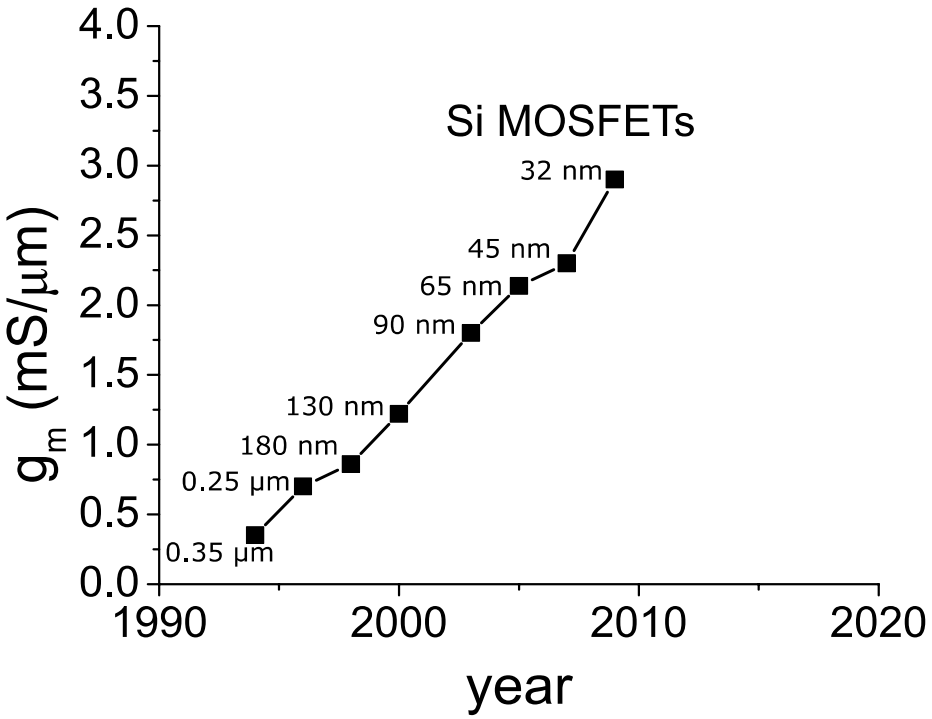


v_{inj}(InGaAs) > 2v_{inj}(Si) at less than half V_{DD}

→ high current at low voltage

Transconductance of Planar Si vs. InGaAs MOSFETs

n-MOSFETs in Intel's nodes at nominal voltage



"Comparisons always fraught with danger…"

Transconductance of Planar Si vs. InGaAs MOSFETs

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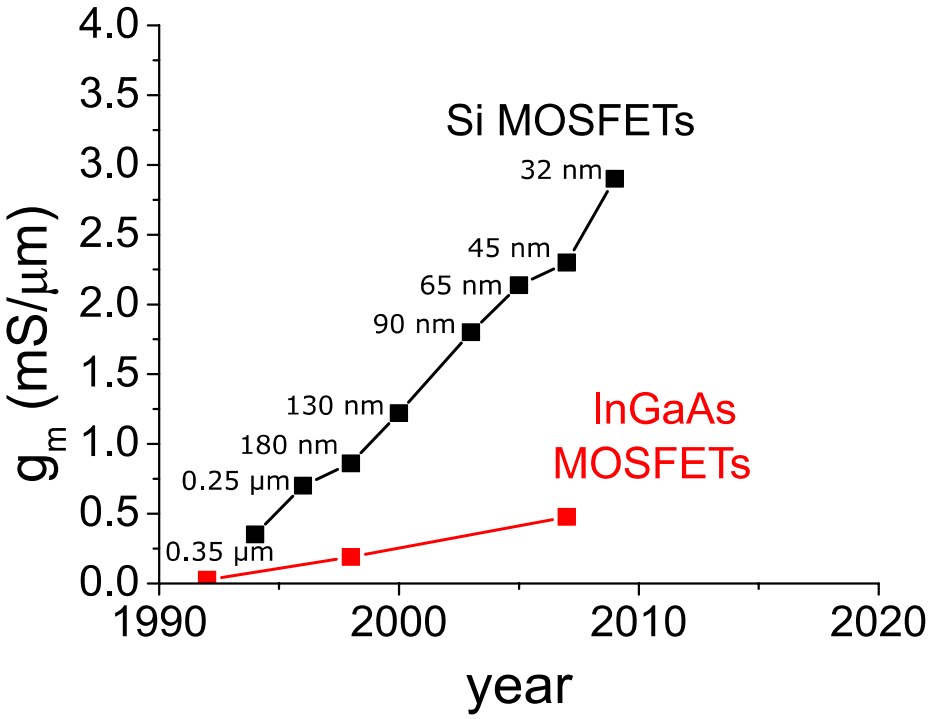
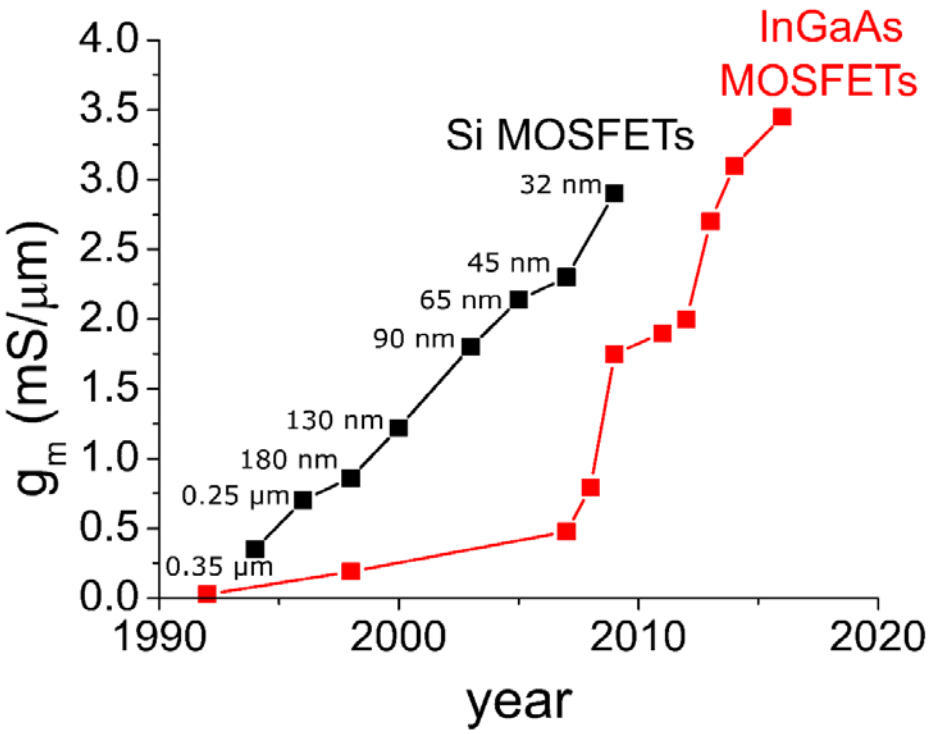


"Comparisons always fraught with danger…"

- InGaAs stagnant for a long time

Transconductance of Planar Si vs. InGaAs MOSFETs

n-MOSFETs in Intel's nodes at nominal voltage

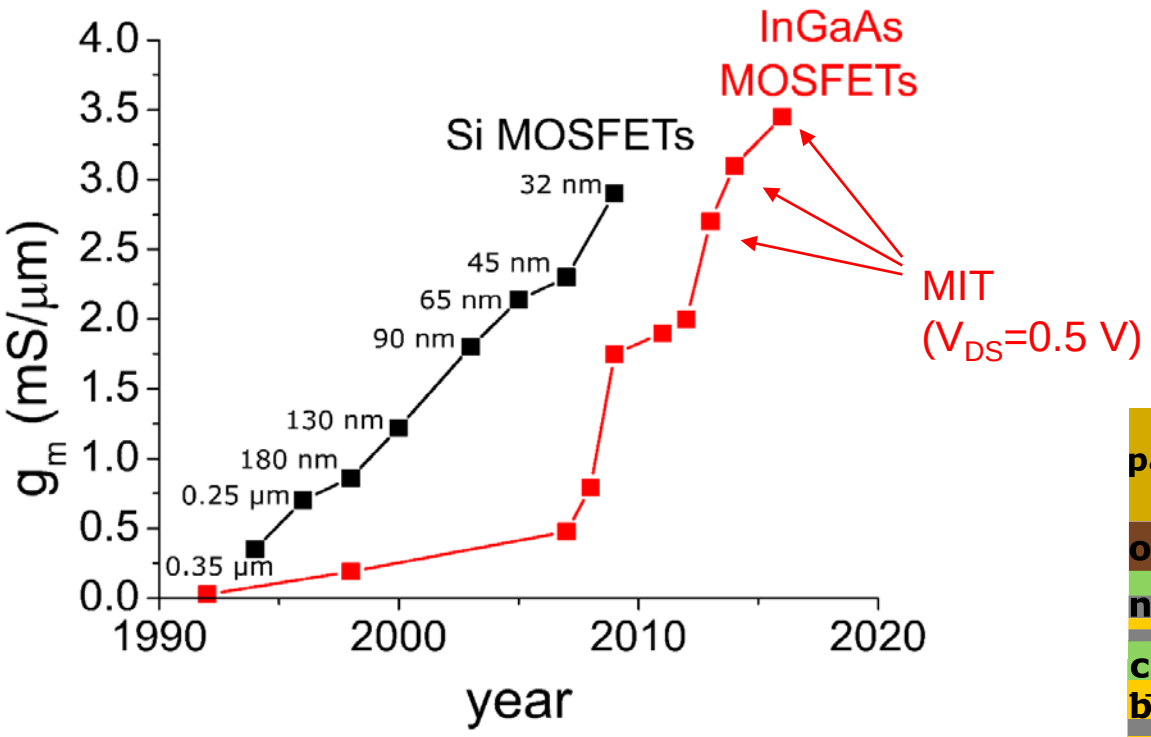


"Comparisons always fraught with danger…"

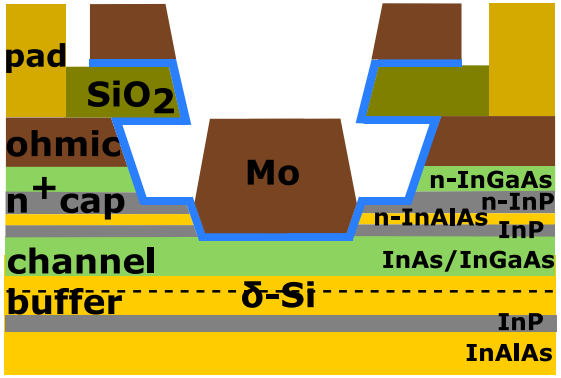
- Rapid recent progress
- InGaAs exceeds Si

Transconductance of Planar Si vs. InGaAs MOSFETs

n-MOSFETs in Intel's nodes at nominal voltage



"Comparisons always fraught with danger…"

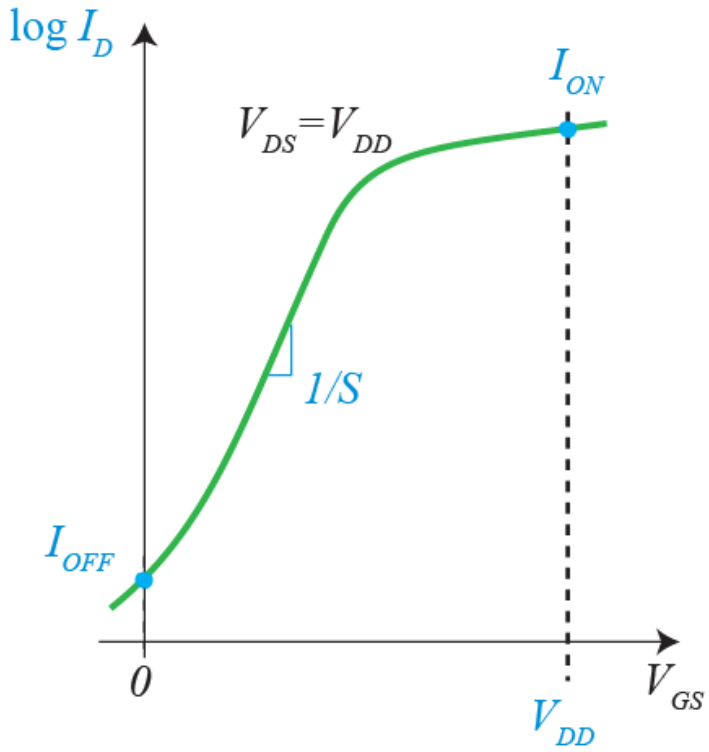


- Rapid recent progress
- InGaAs exceeds Si

Lin,
IEDM 2014
EDL 2016

Many requirements for a successful logic technology

1. ON current
2. OFF current
3. Scalability
4. Stability
5. Manufacturing robustness
6. Si integration



Evolution of transistor structure for improved scalability

Planar bulk MOSFET

Thin-body SOI MOSFET

FinFET

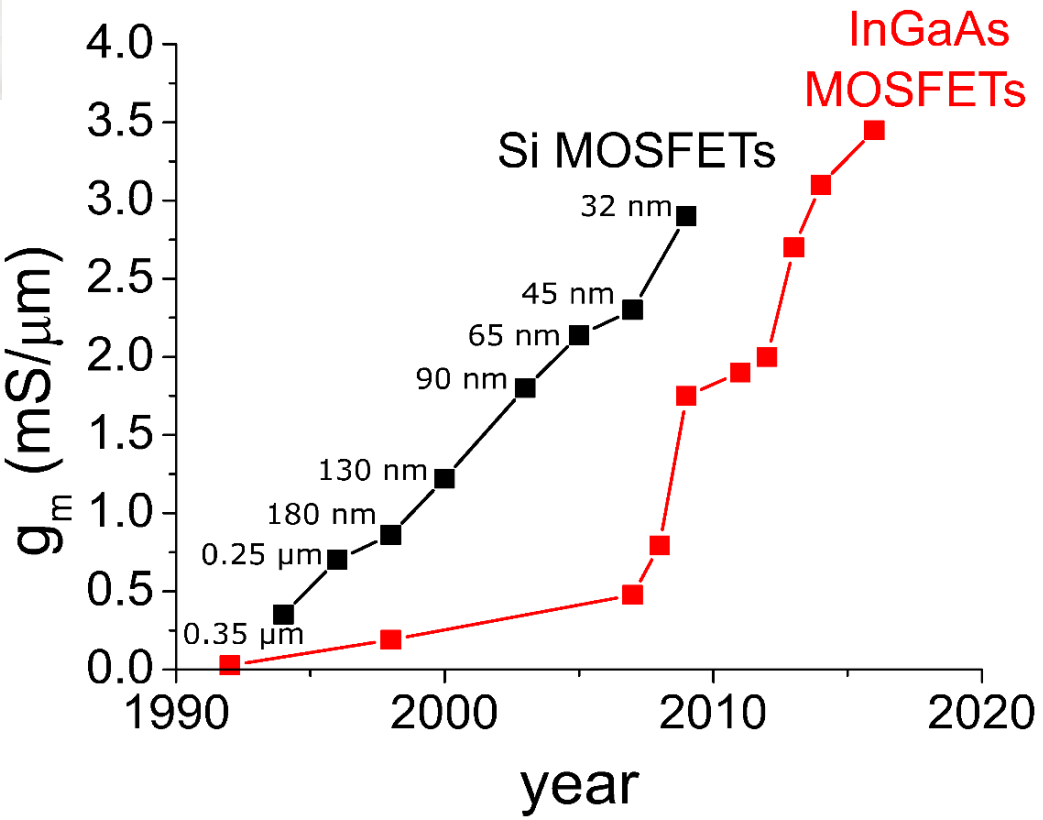
Nanowire MOSFET

Enhanced gate control → improved scalability

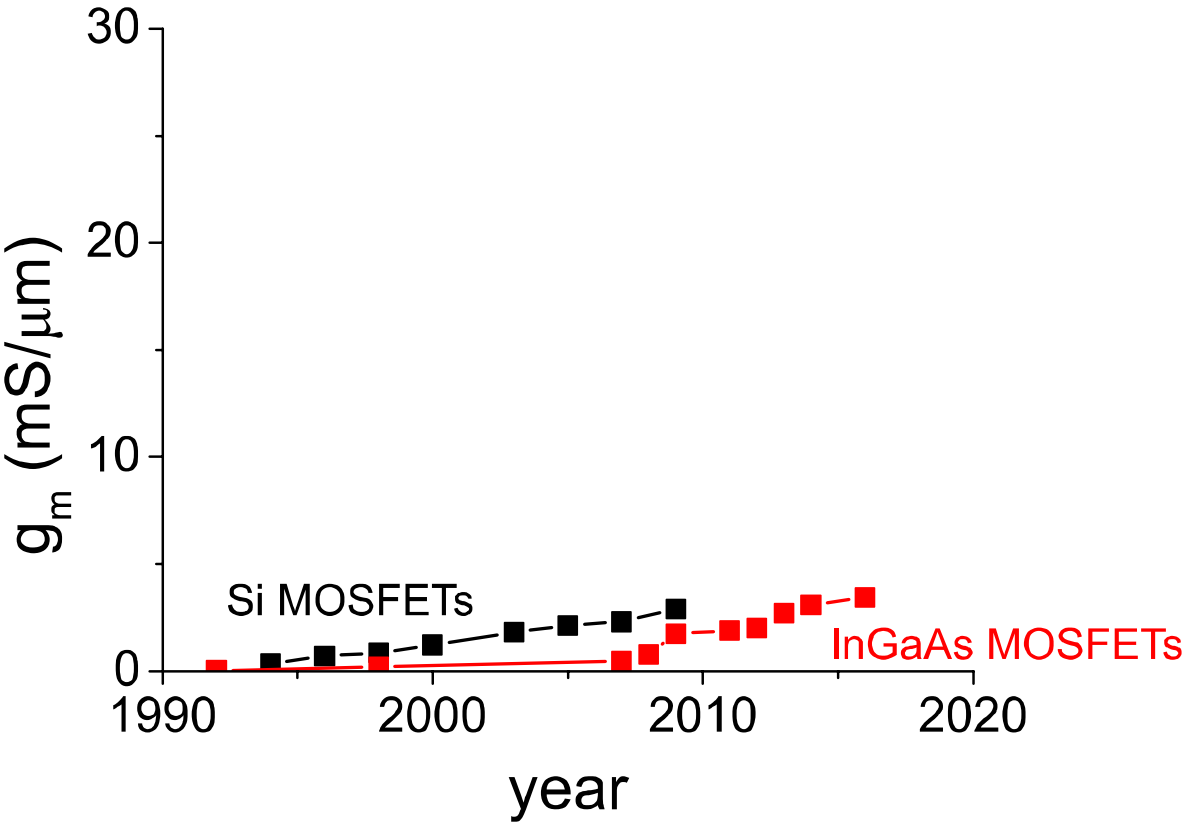
Evolution of transistor structure for improved scalability

Enhanced gate control → improved scalability

Transconductance of planar Si vs. InGaAs MOSFETs



Transconductance of Si vs. InGaAs FinFETs



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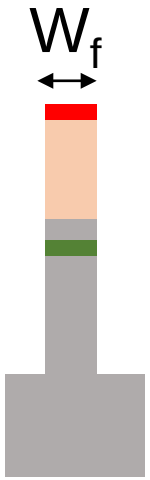
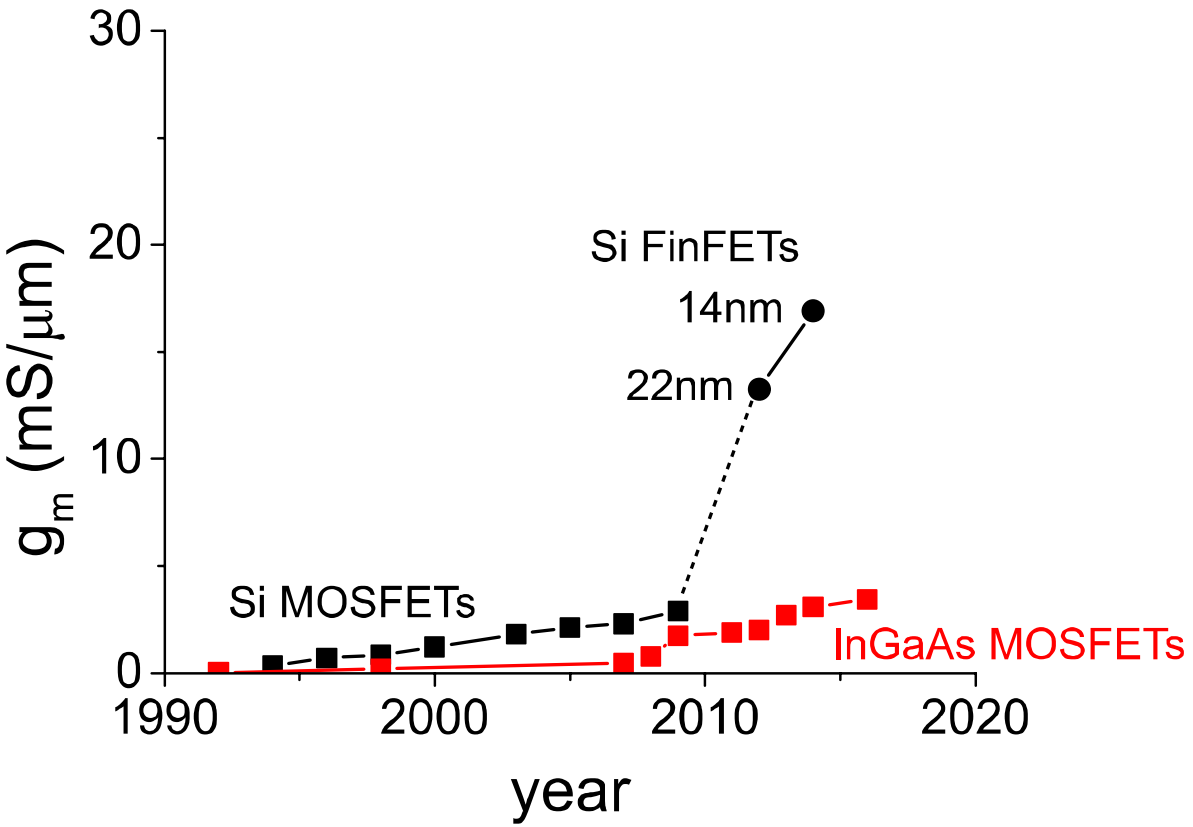
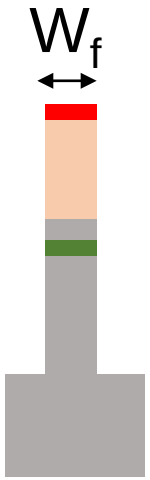


g_m normalized by fin width



FinFET: large increase in current density per unit footprint over planar MOSFET

Transconductance of Si vs. InGaAs FinFETs



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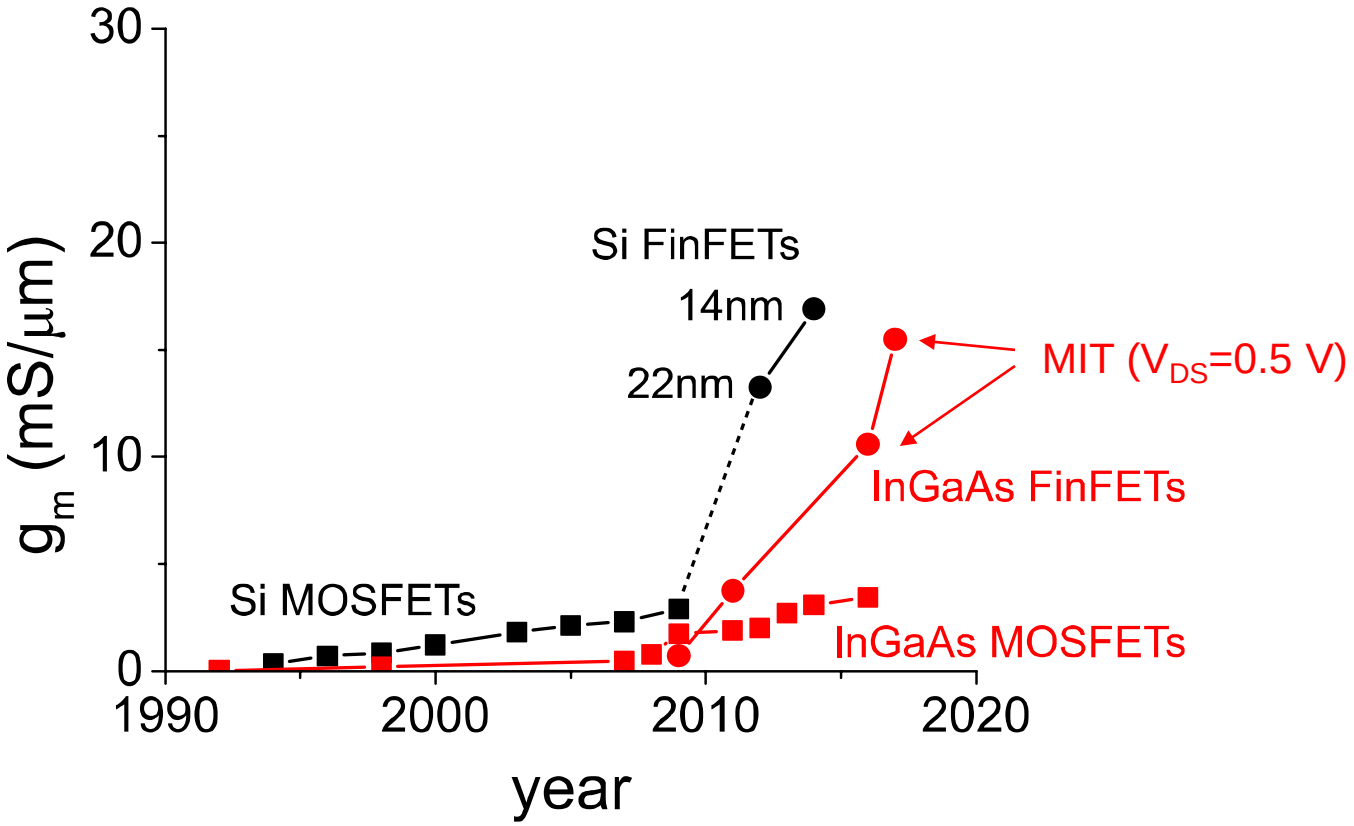
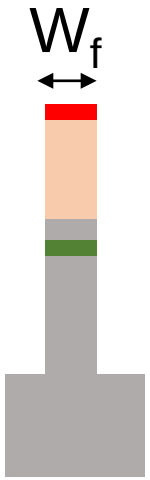


Best InGaAs FinFETs nearly match 14 nm Si MOSFETs

Transconductance of Si vs. InGaAs FinFETs



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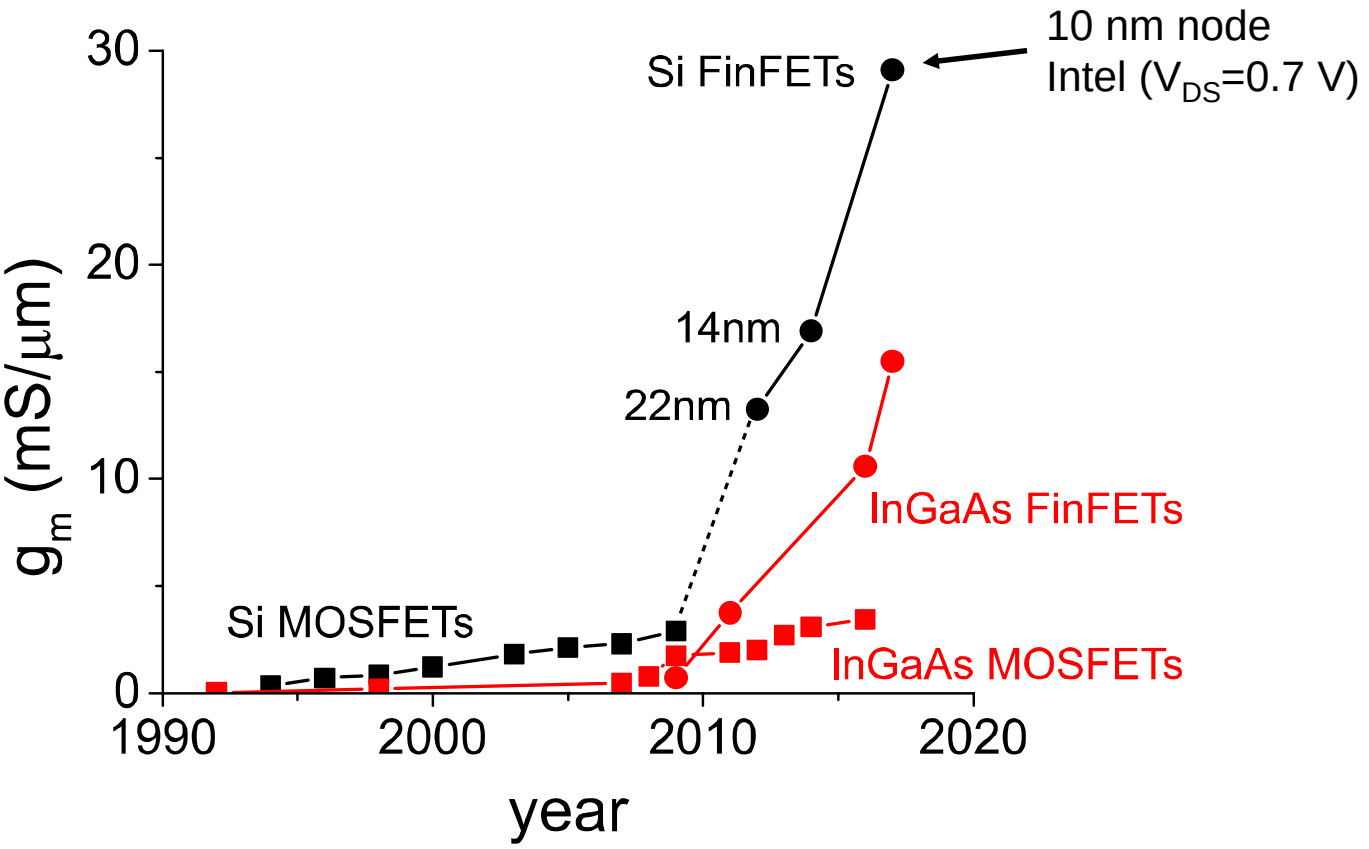
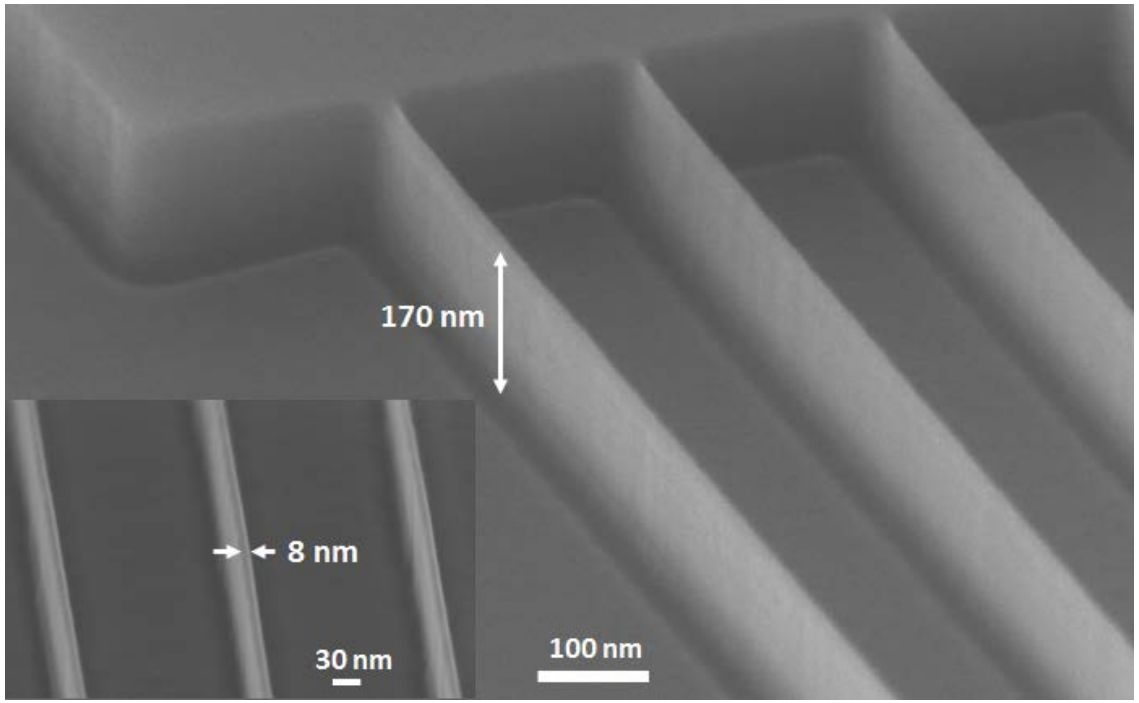


10 nm node Si MOSFETs a great new challenge!

InGaAs FinFETs @ MIT

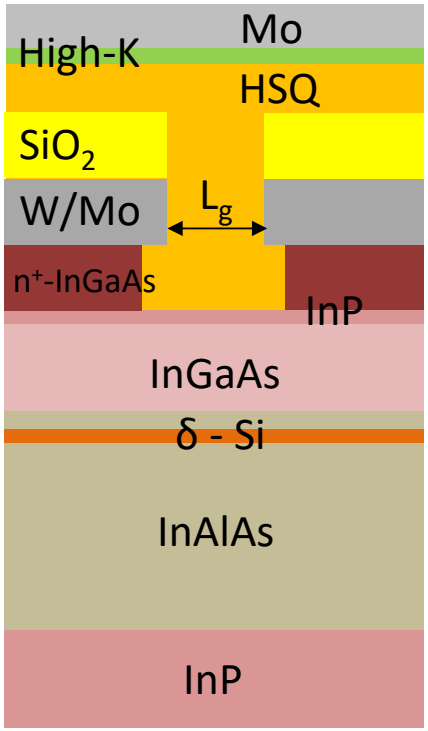
Key enabling technologies: $BCl_3/SiCl_4/Ar$ RIE + digital etch

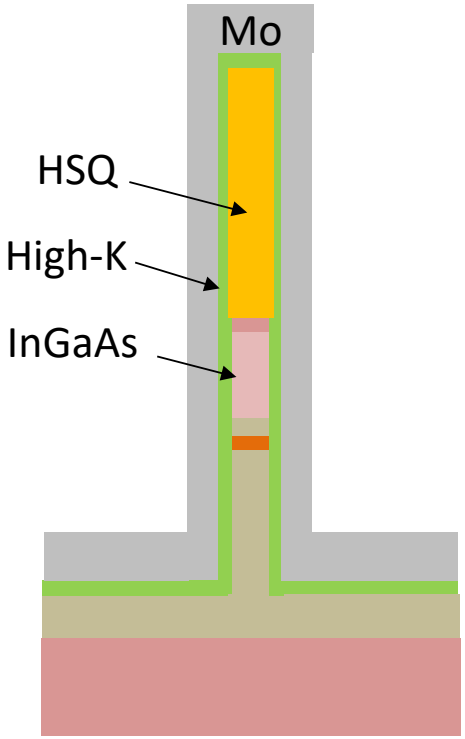


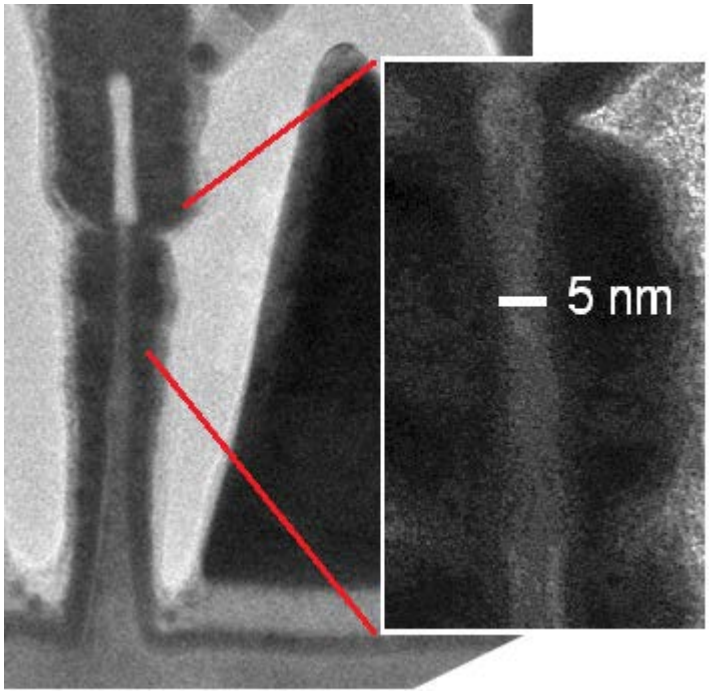
- Sub-10 nm fin width
- Aspect ratio > 20
- Vertical sidewalls

Vardi,
DRC 2014,
EDL 2015,
IEDM 2015

InGaAs FinFETs @ MIT





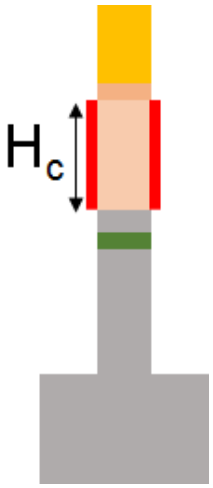


Vardi, IEDM 2017

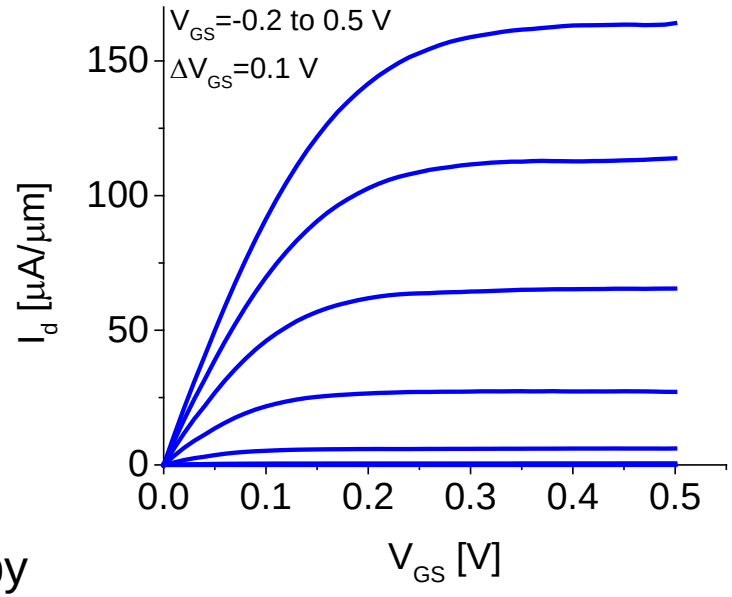
- Si-compatible process
- Contact-first, gate-last process
- Fin etch mask left in place → double-gate MOSFET

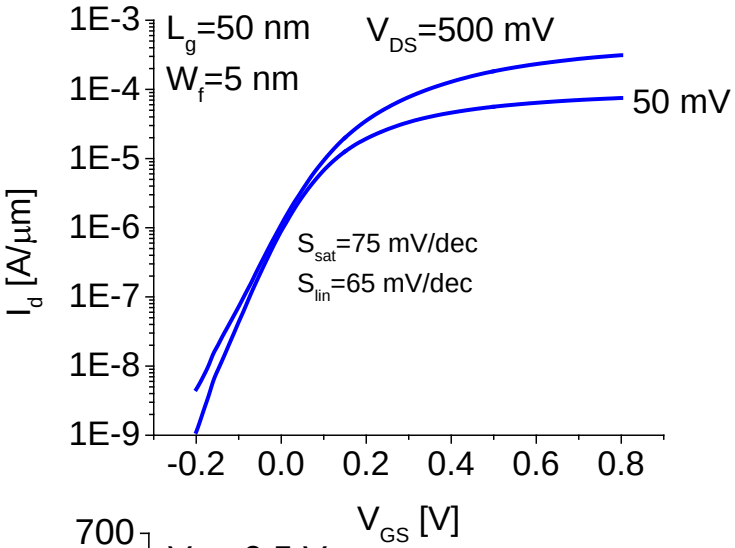
Most aggressively scaled FinFET

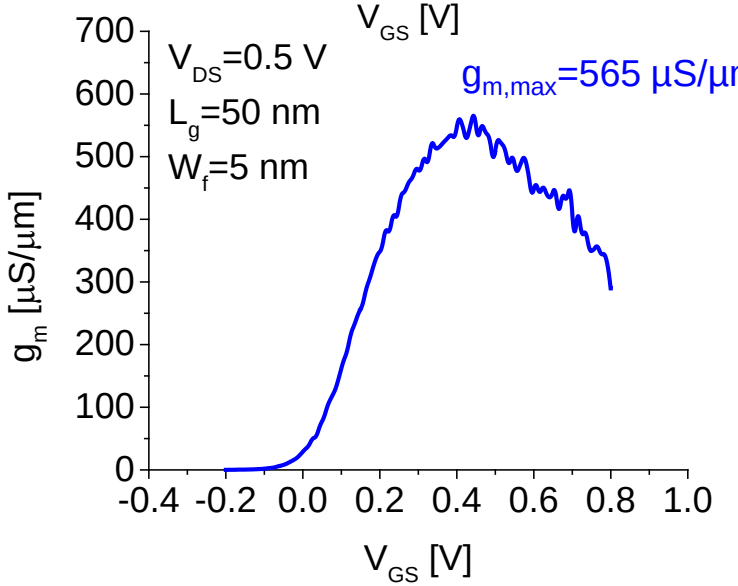
W_f=5 nm, L_g=50 nm, H_c=50 nm (AR=10), EOT=0.8 nm:



Normalized by conducting gate periphery = $2H_c$





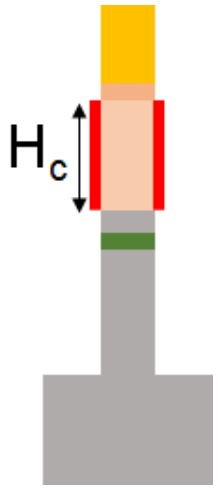


At V_{DS}=0.5 V:

- g_m=565 μS/μm
- R_{on}=660 Ω.μm
- S_{sat}=75 mV/dec
- DIBL=22 mV/V

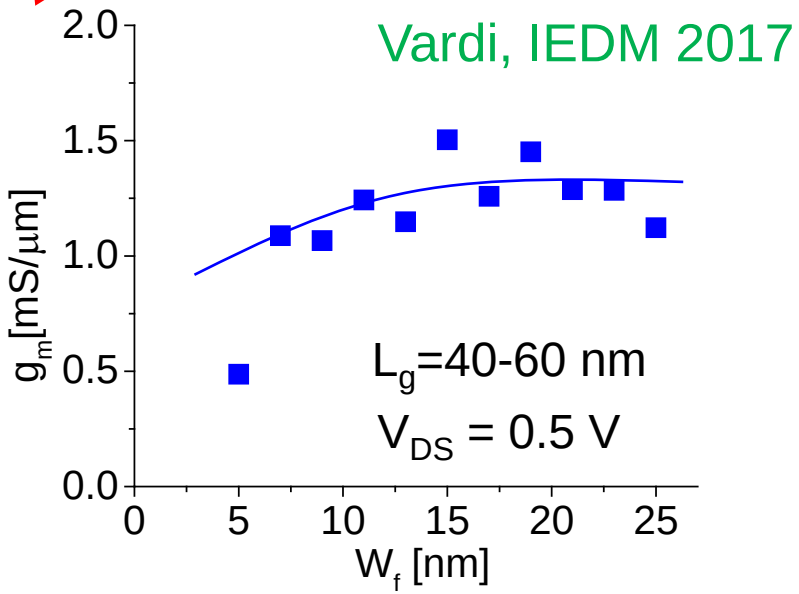
Vardi, IEDM 2017

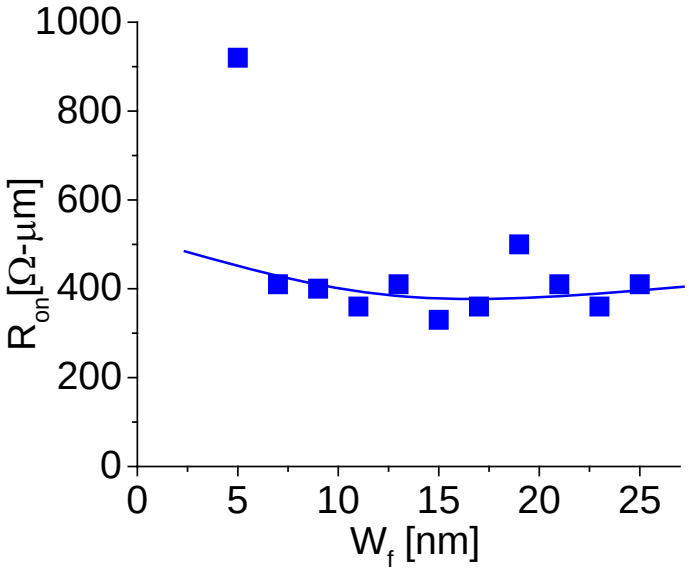
Fin-width scaling of ON-state current



Normalized by conducting gate periphery = $2H_c$

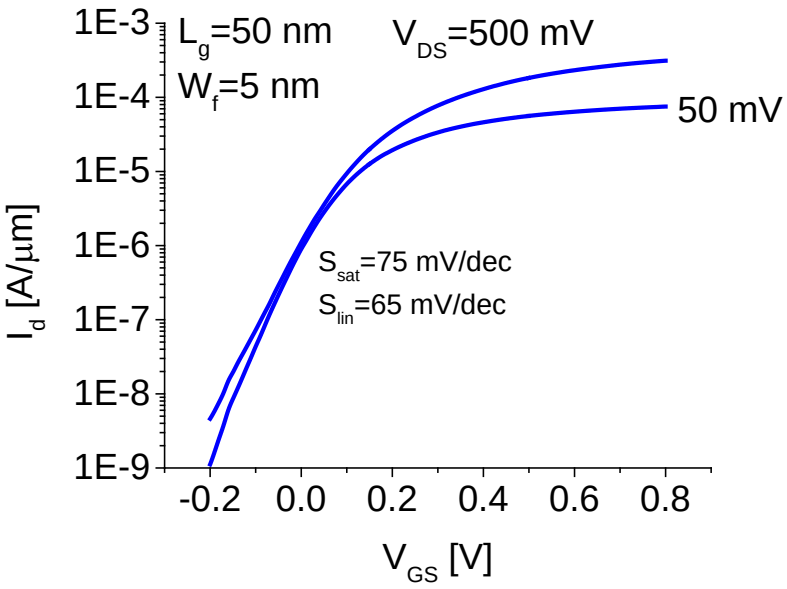
in planar MOSFETs expect 2.2 mS/µm

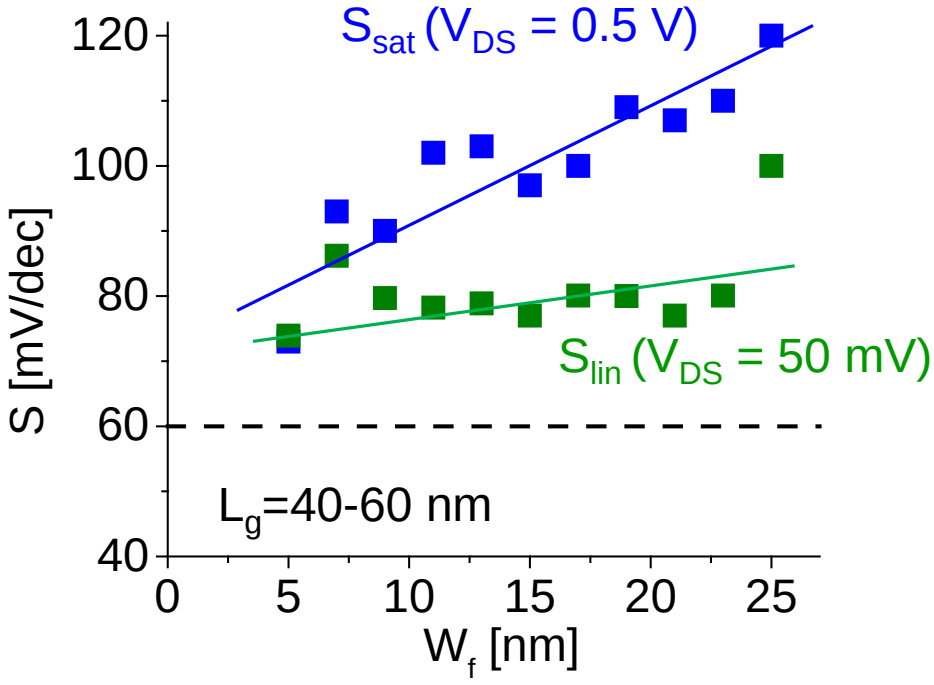




- g_m independent of W_f down to W_f=7 nm
- In planar MOSFET (x=0.53) expect g_m~ 2.2 mS/µm
- Missing performance hints at sidewall damage

Fin-width scaling of OFF-state current



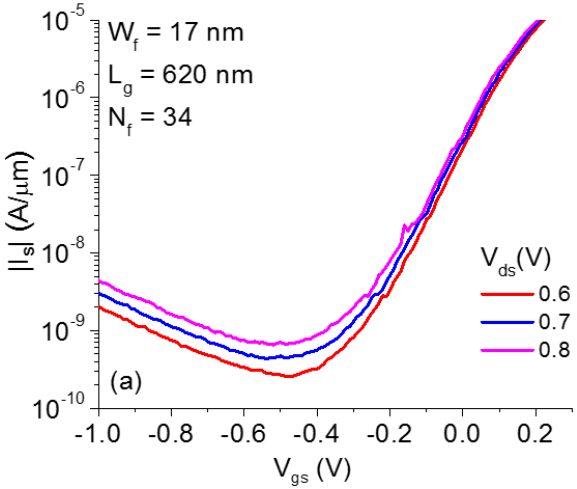


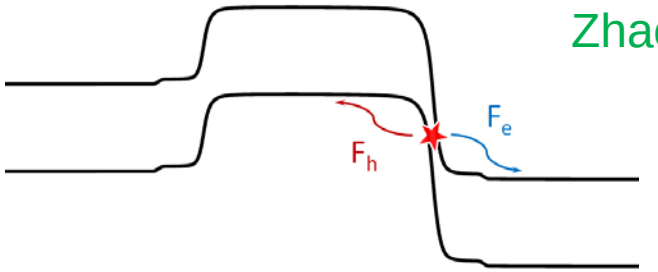
- Excellent subthreshold swing scaling behavior
- From long L_g devices: $D_{it} \sim 8x10^{11}$ $cm^{-2}.eV^{-1}$

Vardi, IEDM 2017

Excess OFF-state current

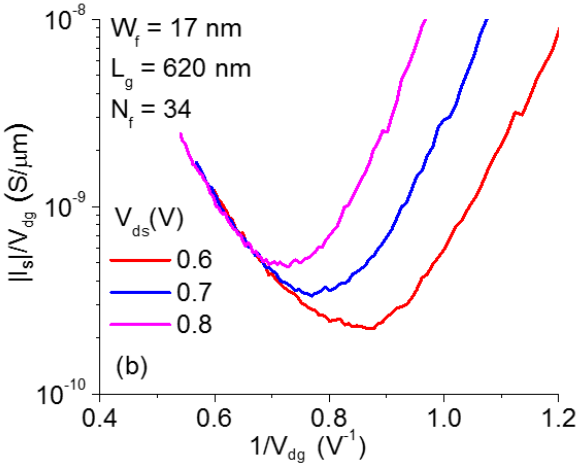
Band-to-band tunneling (BTBT) at drain end of channel

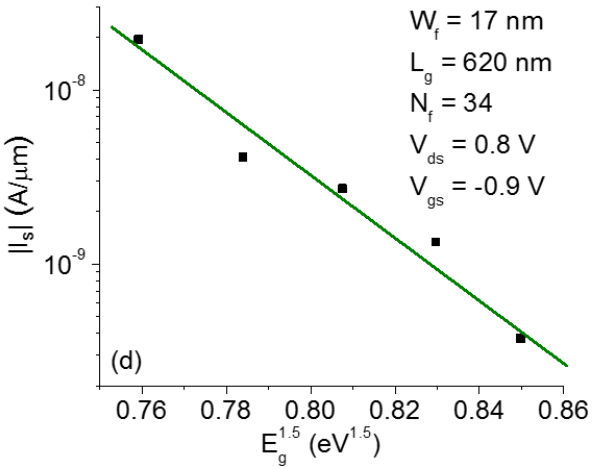




Zhao, EDL 2018

$$|I_{BTBT}| \propto V_{dg} \exp(-A\frac{E_g^{1.5}}{V_{dg}})$$

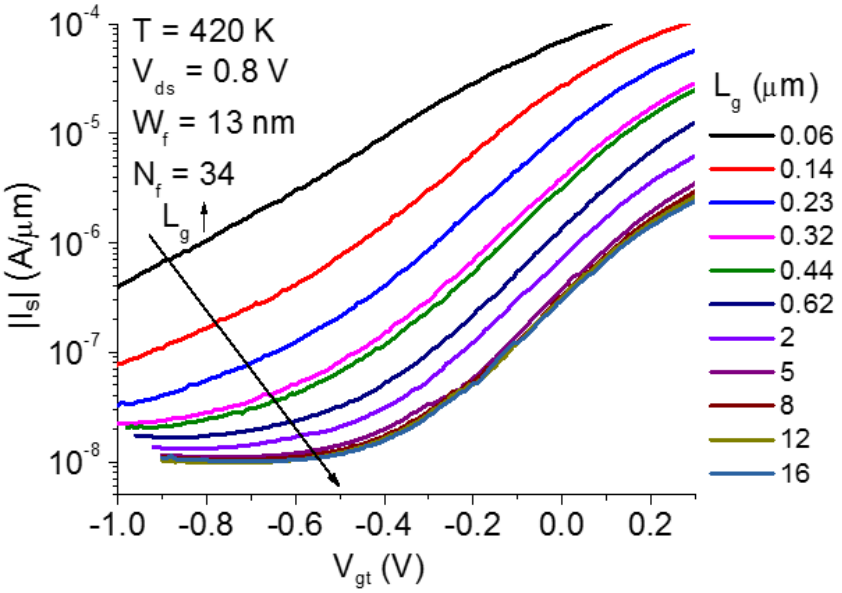


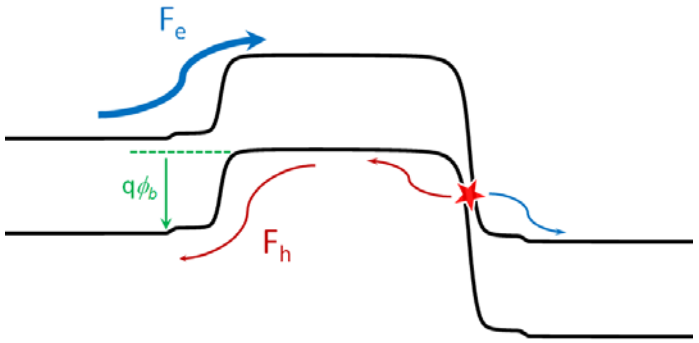


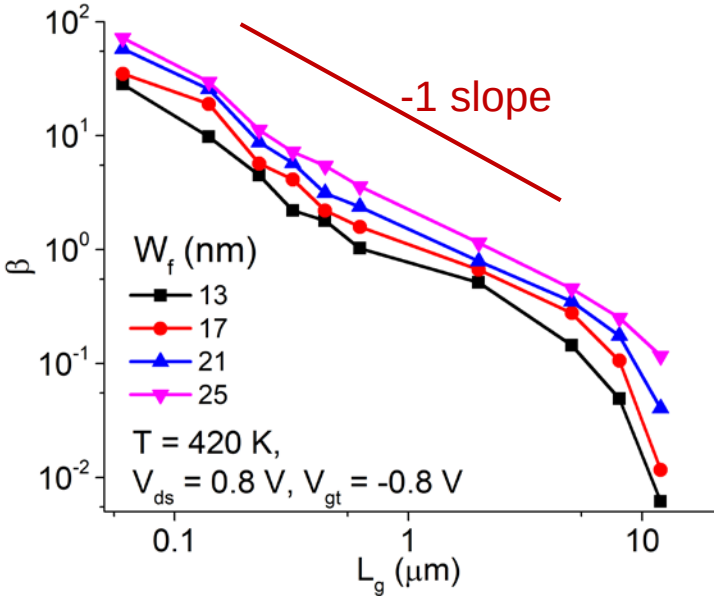
Classic BTBT behavior in long-channel devices

Excess OFF-state current

Current multiplication through *parasitic bipolar transistor*





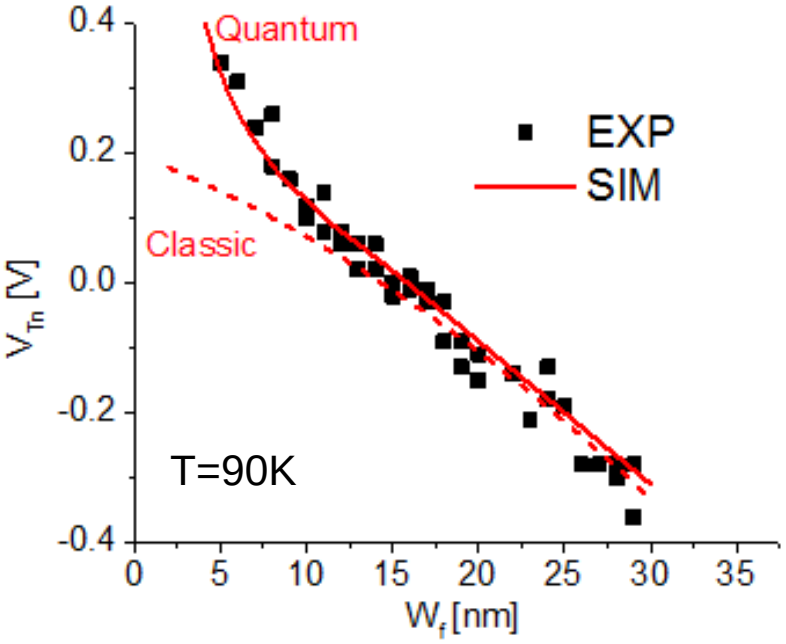


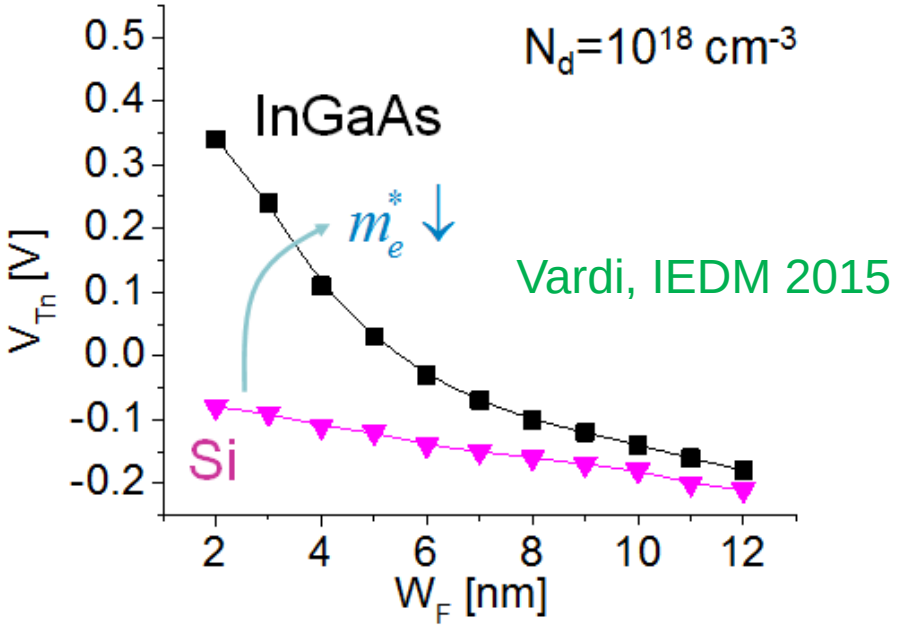
- Large BJT current gain (up to ~100)
- Short L_g: $\beta \sim 1/L_g$
- Long L_g: $\beta \sim \exp(-L_g/L_d)$, $L_d \approx$ 2-4 μm

Zhao, EDL 2018, CSW 2018

Manufacturing robustness: impact of fin width on V_T

InGaAs doped-channel FinFETs: 50 nm thick, $N_D \sim 10^{18}$ cm^{-3}

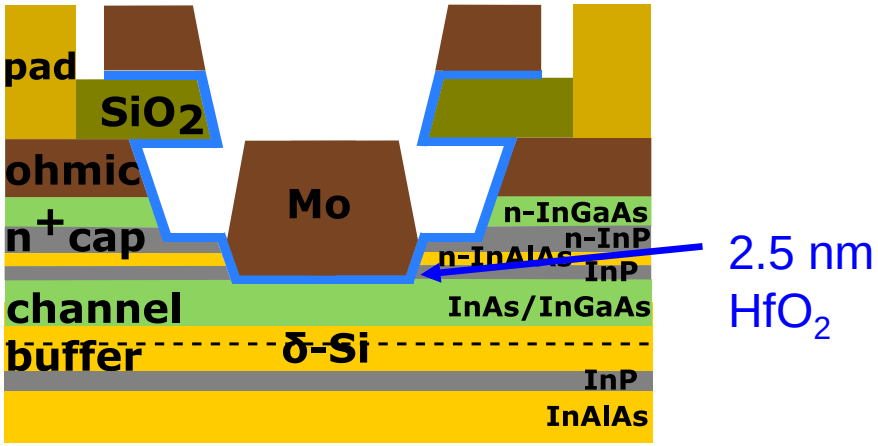


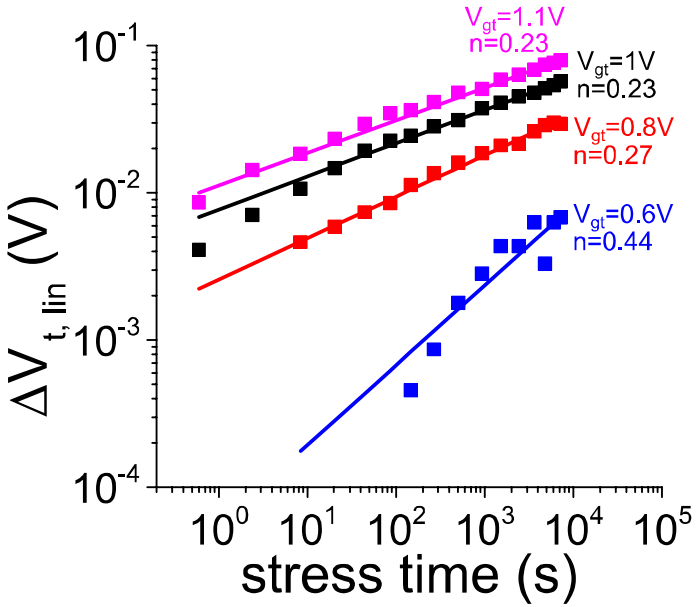


- Strong V_T sensitivity for W_f < 10 nm; much worse than Si
- Due to quantum effects
- Big concern for future manufacturing

MOSFET threshold voltage stability

Planar InGaAs MOSFETs under forward-gate stress (V_{gs}>0):

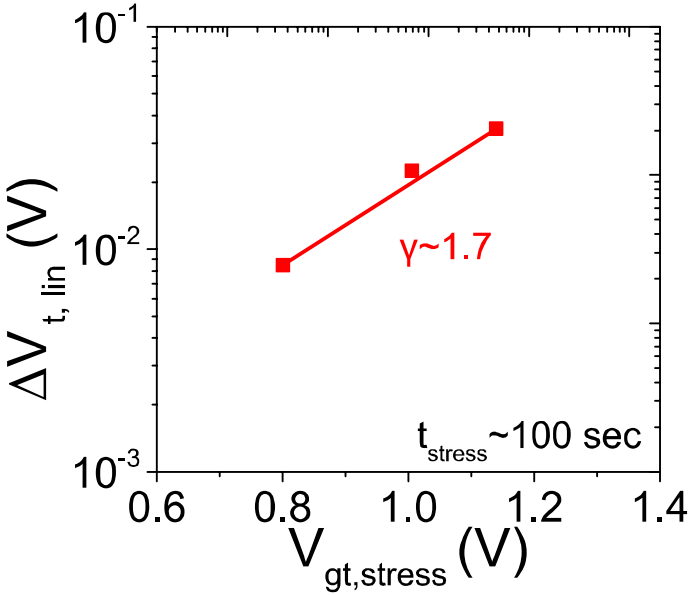




- ΔV_t: power law in time and stress voltage

$$\Delta V_t \propto t_{stress}^{n} (V_{gs} - V_t)^{\gamma}$$

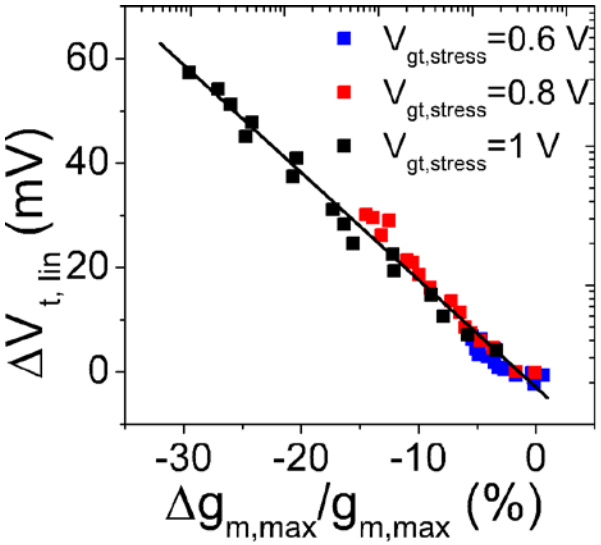
- Typical of PBTI (Positive Bias Stress Instability)

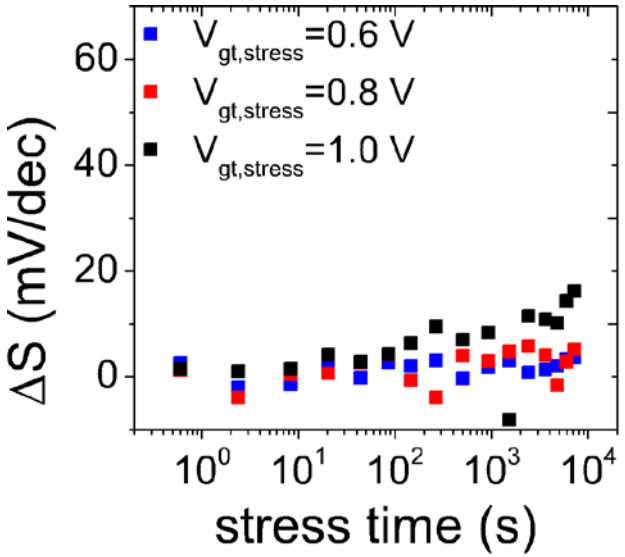


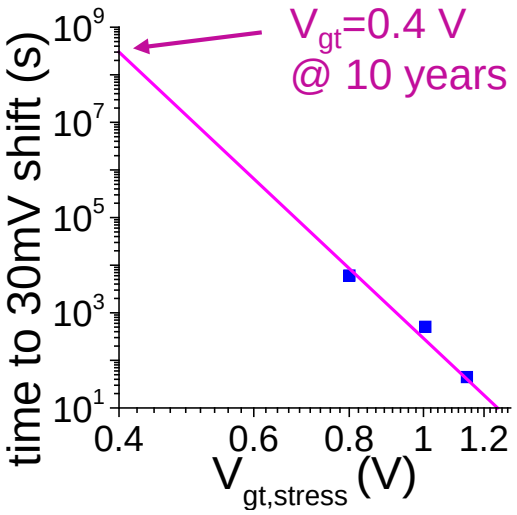
Cai, IEDM 2016

MOSFET stability due to oxide traps

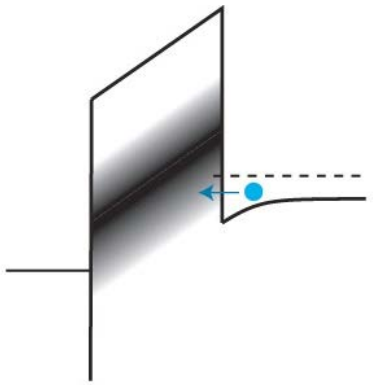
Planar InGaAs MOSFETs under forward-gate stress:







- $\Delta g_{m,max}$ and $\Delta V_{t,lin}$ correlated
- Negligible change in S
- 30 mV shift in 10 years for V_{gt}= 0.4 V
- Oxide traps = O vacancies in HfO_2

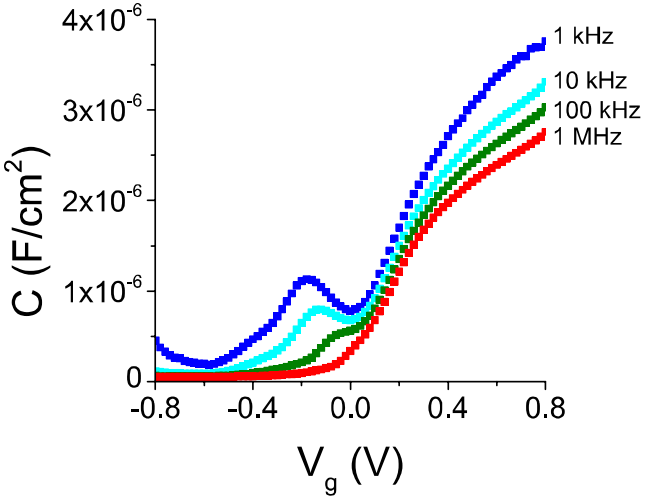


Cai, IEDM 2016

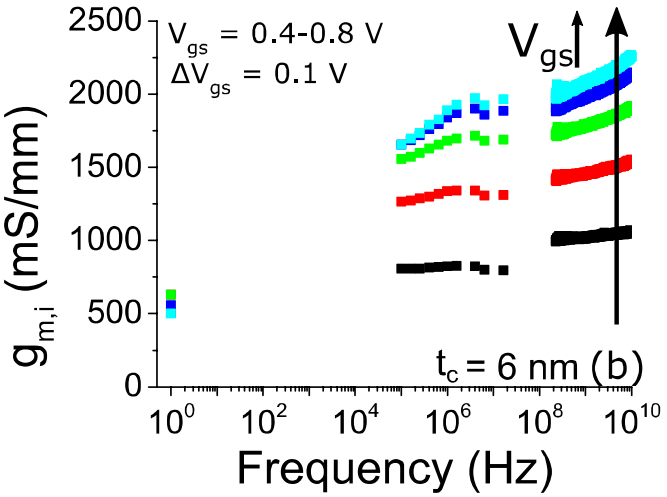
Excellent review by Franco, IEDM 2017

Other manifestations of oxide traps

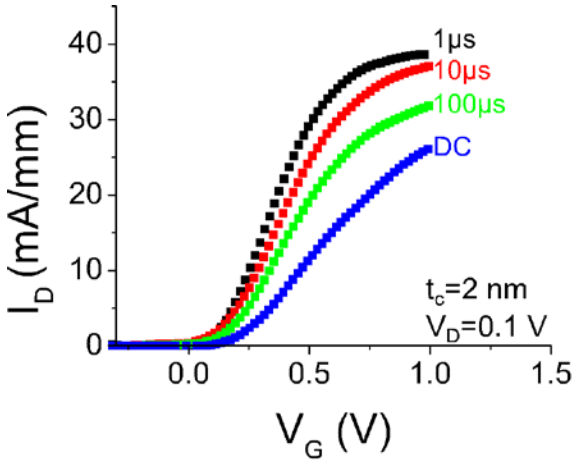
C-V frequency dispersion



g_m frequency dispersion



Pulsed vs. DC



Cai, CSW 2018

Also: Johansson, ESSDERC 2013

- Frequency dispersion in C_g and g_m
- Pulsed I-V ≠ DC I-V
- DC underestimates transistor potential

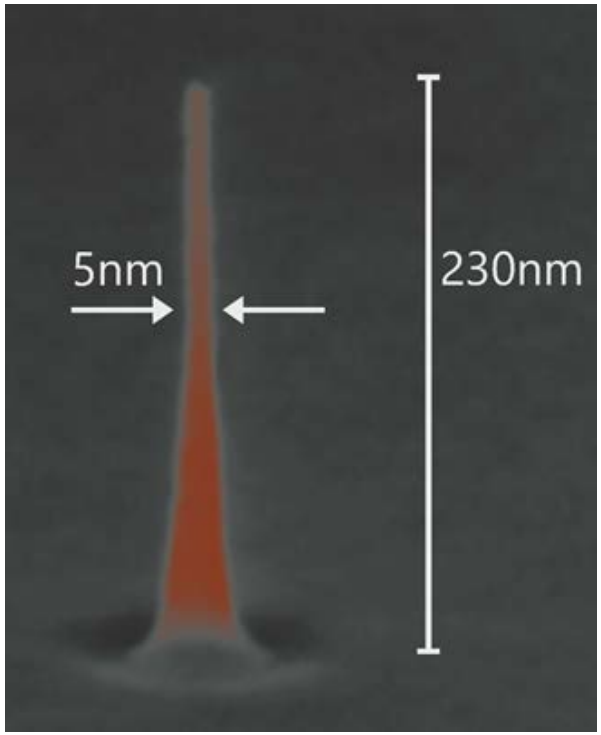
Also: Cartier, ESSDERC 2017

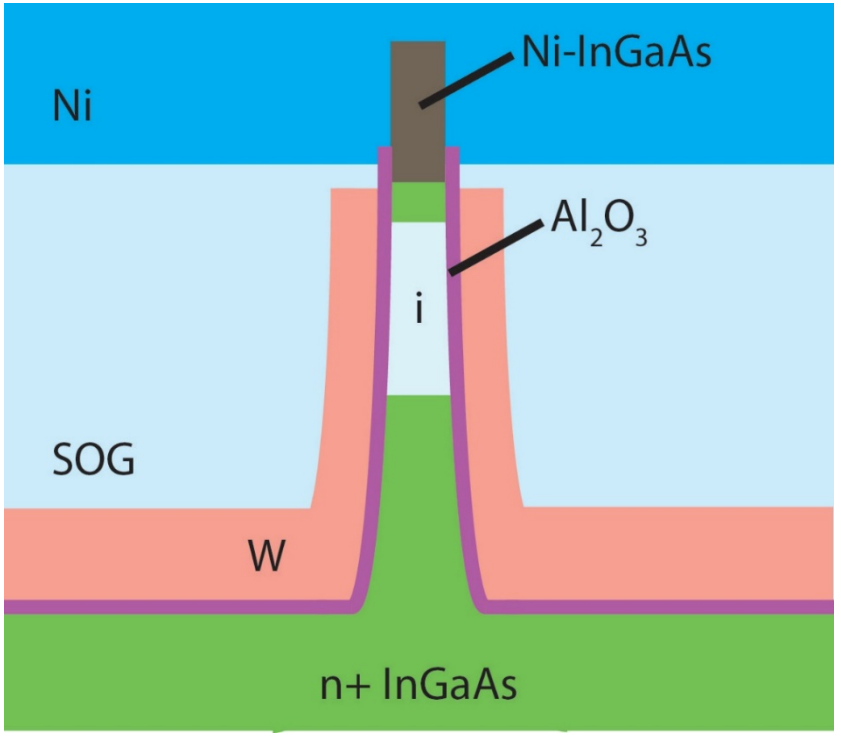
InGaAs Vertical Nanowire MOSFETs

Vertical NW MOSFET:

→ uncouples footprint scaling from L_g, L_{spacer}, and L_c scaling

InGaAs VNW-MOSFETs by top-down approach @ MIT

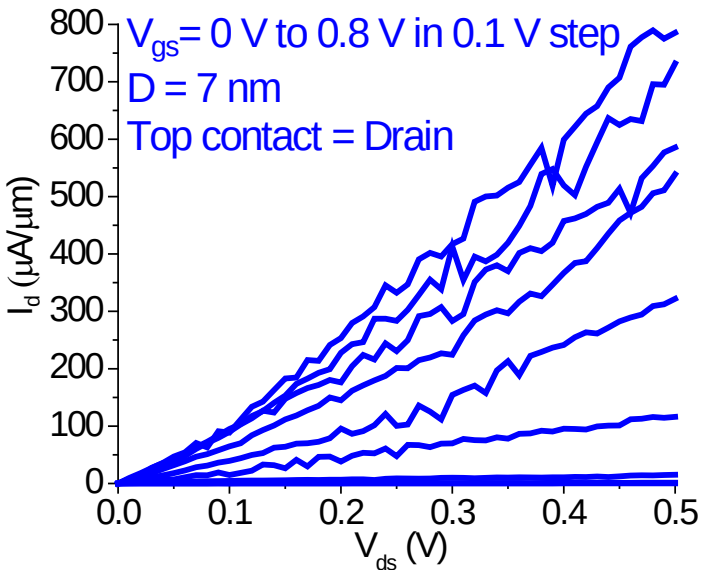


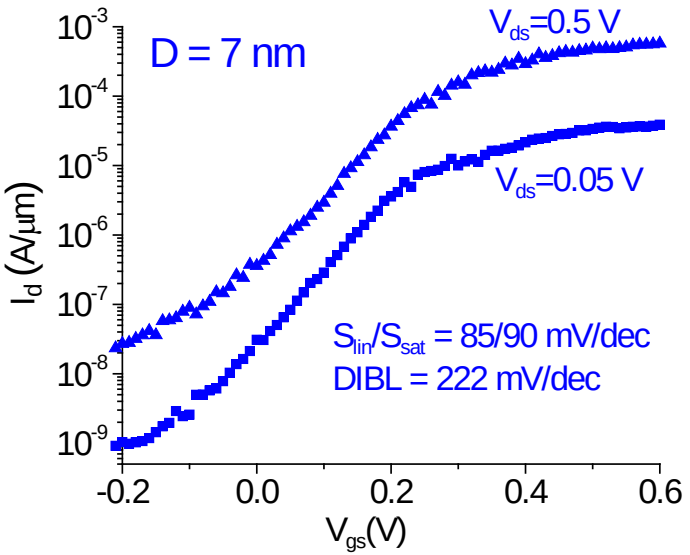


Lu, EDL 2017

- *Top-down* approach: flexible and manufacturable
- Critical technologies: precision RIE + alcohol-based digital etch

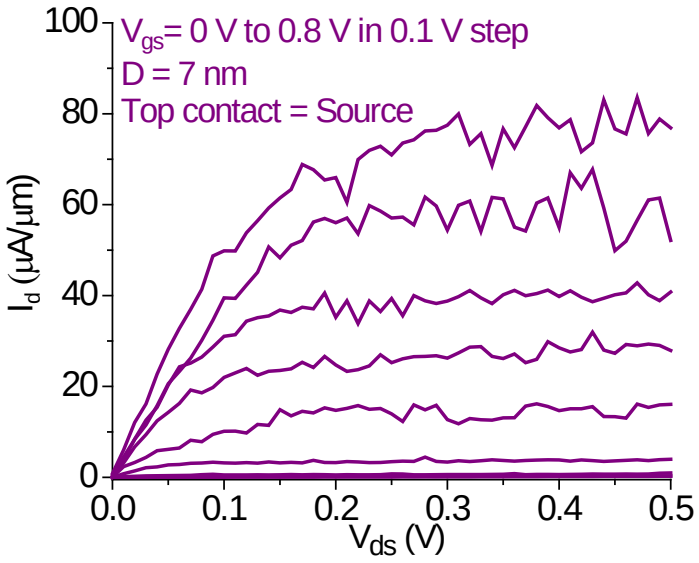
D = 7 nm InGaAs VNW MOSFET





Single nanowire MOSFET:

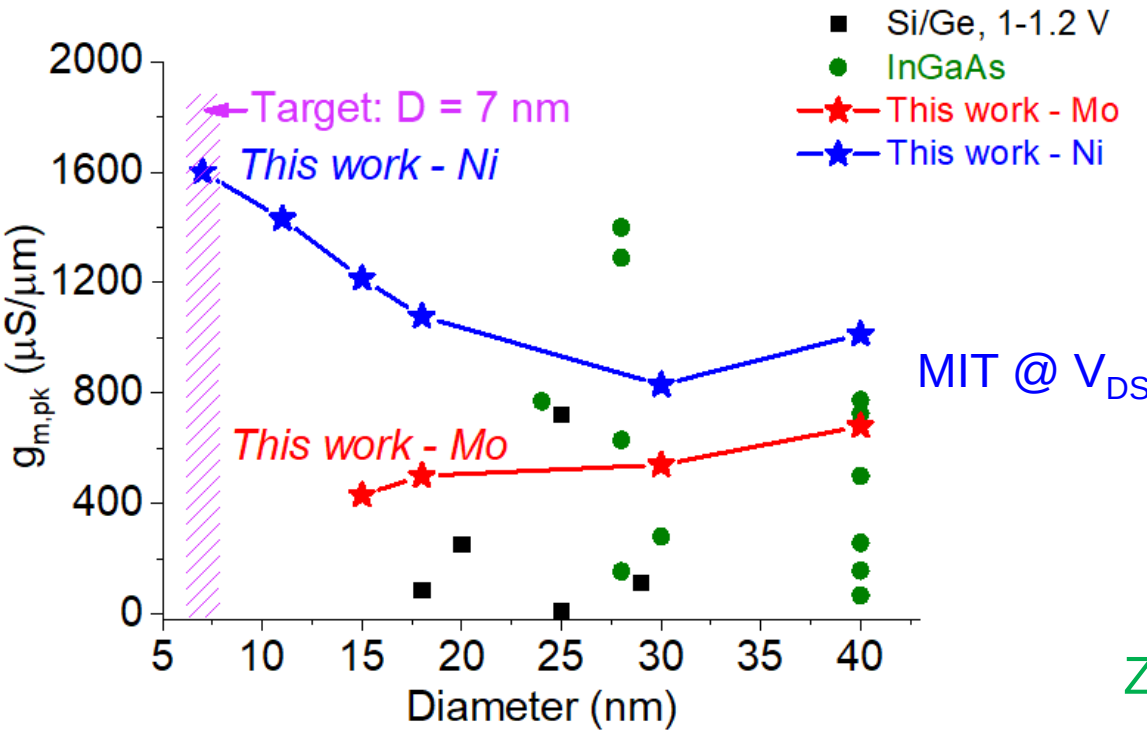
- L_{ch}= 80 nm
- 2.5 nm Al_2O_3 (EOT = 1.3 nm)
- $g_{m,pk}$=1700 μS/μm
- Top contact = key problem



Zhao, IEDM 2017

Benchmark with Si / Ge VNW MOSFETs

Peak g_m of InGaAs (V_{DS}=0.5 V), Si and Ge VNW MOSFETs

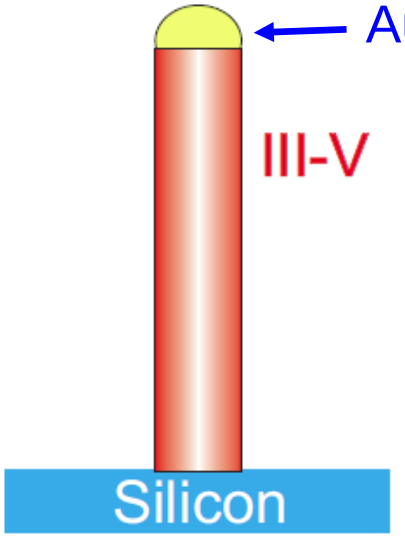


MIT @ V_{DS}=0.5 V

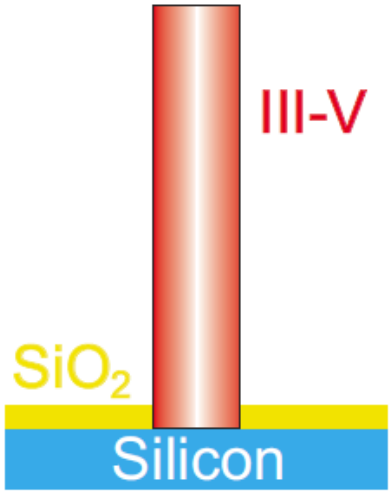
Zhao, IEDM 2017

- First sub-10 nm diameter VNW FET of any kind on any material system
- InGaAs competitive with Si [hard to add strain]

InGaAs Vertical Nanowires on Si by direct growth

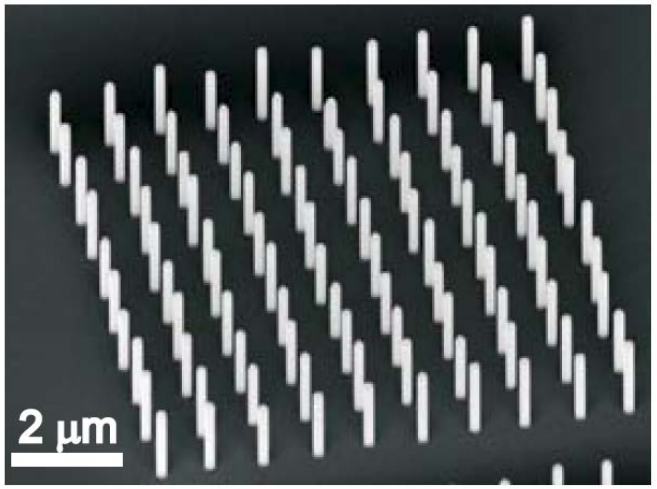


Vapor-Solid-Liquid (VLS) Technique

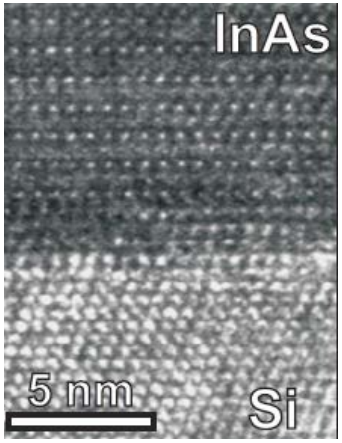


Selective-Area Epitaxy (SAE)

Riel, MRS Bull 2014



InAs NWs on Si by SAE



Riel, IEDM 2012

VNW MOSFETs: path for III-V integration on Si for future CMOS

Conclusions

1. Great recent progress on planar, fin and nanowire InGaAs MOSFETs
2. Device performance still lacking for 3D architecture designs

   → severe oxide trapping masks true transistor potential
3. Serious challenges identified: excess off-current, stability, manufacturability, integration with Si
4. Vertical Nanowire MOSFET: ultimate scalable transistor; integrates well on Si